What I claim is:

1. A sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin, comprising:

an upper mold; and

a lower mold having an area where the semiconductor wafer is mounted, the lower mold having an uneven surface in the area.

2. A sealing apparatus as claimed in claim 1, wherein the uneven surface is formed by an electric discharging process in coarse condition.

3. A sealing apparatus as claimed in claim 2, wherein the area is a first area, the uneven surface is formed within a second area, which is in the first area, and the uneven surface is not formed in the periphery of the first area.

4. A sealing apparatus as claimed in claim 2, wherein the uneven surface has a roughness in a range between 8μm and 12μm.

5. A sealing apparatus as claimed in claim 3, wherein the uneven surface has a roughness in a range between 8μm and 12μm.

6. A sealing apparatus as claimed in claim 1, wherein the uneven surface is formed by slits.

7. A sealing apparatus as claimed in claim 6, wherein the slits are formed in parallel to each other.

8. A sealing apparatus as claimed in claim 6, wherein the area is a first area, the slits is formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

9. A sealing apparatus as claimed in claim 7, wherein the area is a first area, the slits is formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

10. A sealing apparatus as claimed in claim 1, wherein the uneven surface is formed by a single spiral slit.

11. A sealing apparatus as claimed in claim 10, wherein the area is a first area, the single spiral slit is formed within a second area, which is in the first area, and the single spiral slit is not extended to the periphery of the first area.

12. A sealing apparatus as claimed in claim 1, further comprising a shock absorber, which is formed under the lower mold, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and lower molds.

13. A sealing apparatus as claimed in claim 1, further comprising shock absorbers which are formed under the lower mold, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold, the shock absorbers being disposed symmetrically against the center of the area.

14. A sealing apparatus as claimed in claim 12, wherein the shock absorber is formed by a metallic compression spring.

15. A sealing apparatus as claimed in claim 13, wherein each shock absorber is formed by a metallic compression spring.

16. A sealing apparatus as claimed in claim 12, wherein the shock absorber is a first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

17. A sealing apparatus as claimed in claim 12 wherein the shock absorber is a first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

18. A sealing apparatus as claimed in claim 16, wherein the second shock absorber is formed by a metallic compression spring.

19. A sealing apparatus as claimed in claim 17, wherein each second shock absorber is formed by a metallic compression spring.

20. A sealing apparatus as claimed in claim 13, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

21. A sealing apparatus as claimed in claim 13, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

22. A sealing apparatus as claimed in claim 20, wherein the second shock absorber is formed by a metallic compression spring.

23. A sealing apparatus as claimed in claim 21, wherein each second shock absorber is formed by a metallic compression spring.

24. A sealing apparatus as claimed in claim 1, wherein the upper mold includes a main surface and includes a cavity on the main surface, and wherein the

semiconductor wafer is sandwiched at its periphery by the main surface of the upper mold other than an area where the cavity is formed and the lower mold whereby the resin is not formed on the periphery of the semiconductor wafer.

25. A sealing apparatus as claimed in claim 24, wherein the cavity is located at a position corresponding to the area, wherein the upper mold further includes a gate connected to the cavity and cull connected to the gate, wherein the gate is located at a position corresponding the periphery of the semiconductor wafer, and where the cavity is formed deeper than the gate.

26. A sealing apparatus as claimed in claim 25, wherein the width of the gate is expanding toward the cavity.

27. A sealing apparatus as claimed in claim 25, wherein the upper mold includes a air vent, which is located at a position opposite to the gate, for releasing air in the cavity when the semiconductor wafer is sealed.

28. A sealing apparatus as claimed in claim 26, wherein the upper mold includes a air vent, which is located at a position opposite to the gate, for releasing air in the cavity when the semiconductor wafer is sealed.

29. A sealing apparatus as claimed in claim 24, further comprising a projection

member being formed underneath the center of a back surface the lower mold, which is opposite to the uneven surface.

30. A sealing apparatus as claimed in claim 24, further comprising ejection pins formed in the lower mold, the ejection pins pushing the semiconductor wafer up after the semiconductor wafer is sealed by the resin.

31. A sealing apparatus as claimed in claim 30, wherein the ejection pins are disposed symmetrically against the center of the area.

32. A semiconductor device manufacturing mold for setting a semiconductor wafer having semiconductor elements on its surface in order to seal the surface by resin, comprising:

an upper mold; and

a lower mold having an area where the semiconductor wafer is mounted, the lower mold having an uneven surface in the area.

33. A semiconductor device manufacturing mold as claimed in claim 32, wherein the uneven surface is formed by an electric discharging process in coarse condition.

34. A semiconductor device manufacturing mold as claimed in claim 33, wherein

the area is a first area, the uneven surface is formed within a second area, which is in the first area, and the uneven surface is not formed in the periphery of the first area.

35. A semiconductor device manufacturing mold as claimed in claim 33, wherein wherein the uneven surface has a roughness in a range between 8μm and 12μm.

36. A semiconductor device manufacturing mold as claimed in claim 34, wherein the uneven surface has a roughness in a range between 8μm and 12μm.

37. A semiconductor device manufacturing mold as claimed in claim 32, wherein the uneven surface is formed by slits.

38. A semiconductor device manufacturing mold as claimed in claim 37, wherein the slits are formed in parallel to each other.

39. A semiconductor device manufacturing mold as claimed in claim 37, wherein the area is a first area, the slits is formed within a second area, which is in the first area, and the slits are not extended to the periphery of the first area.

40. A semiconductor device manufacturing mold as claimed in claim 38, wherein the area is a first area, the slits is formed within a second area, which is in the first

area, and the slits are not extended to the periphery of the first area.

41. A semiconductor device manufacturing mold as claimed in claim 32, wherein the uneven surface is formed by a single spiral slit.

42. A semiconductor device manufacturing mold as claimed in claim 41, wherein the area is a first area, the single spiral slit is formed within a second area, which is in the first area, and the single spiral slit is not extended to the periphery of the first area.

43. A gate of a sealing device having a mold in which a semiconductor wafer having semiconductor elements on its surface is set in order to form a resin layer on the semiconductor wafer by introducing a melted resin from a resin supplier, the gate introducing the melted resin into the mold from a part of a periphery of the semiconductor wafer, and a depth of the gate is lower than the thickness of the resin layer.

44. A gate as claimed in claim 43, wherein a width of the gate is expanding from the resin supplier toward the semiconductor wafer.

45. A sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin, comprising:

an upper mold;

a lower mold having an area where the semiconductor wafer is mounted; and

a shock absorber, which is formed under the lower mold, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and lower molds.

46. A sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin, comprising:

an upper mold;

a lower mold having an area where the semiconductor wafer is mounted; and

shock absorbers, which are formed under the lower mold, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold, the shock absorbers being disposed symmetrically against the center of the area.

47. A sealing apparatus as claimed in claim 45, wherein the shock absorber is formed by a metallic compression spring.

48. A sealing apparatus as claimed in claim 46, wherein each shock absorber is formed by a metallic compression spring.

49. A sealing apparatus as claimed in claim 45, wherein the shock absorber is a

first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

50. A sealing apparatus as claimed in claim 45, wherein the shock absorber is a first shock absorber, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

51. A sealing apparatus as claimed in claim 49, wherein the second shock absorber is formed by a metallic compression spring.

52. A sealing apparatus as claimed in claim 50, wherein each second shock absorber is formed by a metallic compression spring.

53. A sealing apparatus as claimed in claim 46, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

a second shock absorber, which is formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

54. A sealing apparatus as claimed in claim 46, wherein the shock absorbers are first shock absorbers, further comprising:

a first block having a first recess, the lower mold being contained in the first recess;

a second block having a second recess, the first block being contained in the second recess; and

second shock absorbers, which are formed under the second block, buffering stress from the upper mold when the semiconductor wafer is sandwiched by the upper and the lower mold.

55. A sealing apparatus as claimed in claim 53, wherein the second shock absorber is formed by a metallic compression spring.

56. A sealing apparatus as claimed in claim 54, wherein each second shock absorber is formed by a metallic compression spring.

57. A method of manufacturing the semiconductor device, comprising:

preparing a mold having a upper mold and a lower mold, the lower mold having an area where the semiconductor wafer is mounted, the lower mold having an uneven surface in the area, the upper mold having a resin passage for introducing a melted resin on the semiconductor wafer;

setting the semiconductor wafer in the mold;

sandwiching the semiconductor wafer by the upper and lower molds;

introducing the melted resin through the resin passage on the surface of the semiconductor wafer whereby the surface of the semiconductor wafer is sealed by the resin; and

separating the resin sealed semiconductor wafer from the mold.

58. A method of manufacturing the semiconductor device as claimed in claim 57, wherein sandwiching the semiconductor wafer by the upper and lower molds is performed by moving up the lower mold on which the semiconductor wafer is

mounted, in order to contact to the upper mold, which is not moveable.

59. A method of manufacturing the semiconductor device as claimed in claim 57, wherein separating the resin sealed semiconductor wafer from the mold includes separating the sealed semiconductor wafer from the upper mold by moving the lower mold down, and separating the sealed semiconductor wafer from the lower mold by pushing the sealed semiconductor wafer up.

60. A method of manufacturing the semiconductor device as claimed in claim 57, wherein the uneven surface is formed in a coarse condition by an electric discharging process.

61. A method of manufacturing the semiconductor device as claimed in claim 60, wherein the area is a first area, the coarse surface is formed within a second area, which is in the first area, and the coarse surface is not formed in the periphery of the first area.

62. A method of manufacturing the semiconductor device as claimed in claim 61, wherein the coarse surface has a roughness in a range between 8μm and 12μm.

63. A method of manufacturing the semiconductor device as claimed in claim 61, further including polishing the resin, which seals the semiconductor wafer, after the

semiconductor wafer is separated from the mold.

64. A method of manufacturing the semiconductor device as claimed in claim 57, wherein when the semiconductor wafer is sandwiched by the upper and lower molds, the upper and lower molds sandwich the periphery of the semiconductor wafer in order not to seal the periphery of the semiconductor wafer by the resin while the melted resin is introduced on the semiconductor wafer.

65. A method of manufacturing the semiconductor device as claimed in claim 64, wherein the semiconductor wafer includes grid lines on its surface for identifying independent semiconductor devices so that parts of the grid lines are exposed after the resin sealed semiconductor wafer is separated from the mold.

66. A method of manufacturing the semiconductor device as claimed in claim 65, further comprising cutting the semiconductor wafer along the grid lines to form the independent semiconductor devices after the resin is polished.

67. A method of manufacturing the semiconductor device having a lower mold and an upper mold, comprising:

introducing the melted resin on the surface of a semiconductor wafer while the semiconductor wafer is sandwiched by the upper and lower molds; and

buffering stress caused by the lower mold and the upper mold and applied to

the semiconductor wafer during introducing the melted resin on the surface of a semiconductor wafer and during sandwiching the semiconductor wafer.

68. A method of manufacturing the semiconductor device as claimed in claim 67, wherein stress is buffered by at least one shock absorber, which is formed under the lower mold.

69. A method of manufacturing the semiconductor device, comprising:

preparing a mold having a upper mold and a lower mold, the lower mold having an area where the semiconductor wafer is mounted, the upper mold having a resin passage for introducing a melted resin on the semiconductor wafer;

setting the semiconductor wafer in the mold;

sandwiching the semiconductor wafer by the upper and lower molds;

introducing the melted resin through the resin passage on a main surface of the semiconductor wafer whereby the surface of the semiconductor wafer is sealed by the resin;

separating the sealed semiconductor wafer from the upper mold by moving the lower mold down; and

separating the resin sealed semiconductor wafer from the lower mold.

70. A method of manufacturing the semiconductor device as claimed in claim 69, wherein sandwiching the semiconductor wafer by the upper and lower molds is

performed by moving up the lower mold on which the semiconductor wafer is mounted, in order to contact to the upper mold, which is not moveable

71. A method of manufacturing the semiconductor device as claimed in claim 69, wherein the sealed semiconductor wafer is separated from the lower mold by pushing the sealed semiconductor wafer up under the condition that the resin on the semiconductor wafer is connected to the other resin formed in a part of the resin passage.

72. A method of manufacturing the semiconductor device as claimed in claim 71, further comprising detaching the other resin formed in the part of the resin passage from the resin formed on the semiconductor wafer after the sealed semiconductor wafer is separated from the lower mold by pushing the sealed semiconductor wafer up.

73. A method of manufacturing the semiconductor device as claimed in claim 69, wherein when the semiconductor wafer is sandwiched by the upper and lower molds, the upper and lower molds sandwich the periphery of the semiconductor wafer in order not to seal the periphery of the semiconductor wafer by the resin while the melted resin is introduced on the semiconductor wafer.

74. A method of manufacturing the semiconductor device as claimed in claim 70,

wherein when the semiconductor wafer is sandwiched by the upper and lower molds, the upper and lower molds sandwich the periphery of the semiconductor wafer in order not to seal the periphery of the semiconductor wafer by the resin while the melted resin is introduced on the semiconductor wafer.

75. A method of manufacturing the semiconductor device as claimed in claim 73, wherein the semiconductor wafer includes grid lines on its surface for identifying independent semiconductor devices so that parts of the grid lines are exposed after the resin sealed semiconductor wafer is separated from the mold.

76. A method of manufacturing the semiconductor device as claimed in claim 74, wherein the semiconductor wafer includes grid lines on its surface for identifying independent semiconductor devices so that parts of the grid lines are exposed after the resin sealed semiconductor wafer is separated from the mold.

77. A method of manufacturing the semiconductor device as claimed in claim 75, further comprising polishing the resin, which seals the semiconductor wafer, after the semiconductor wafer is separated from the mold.

78. A method of manufacturing the semiconductor device as claimed in claim 76, further comprising polishing the resin, which seals the semiconductor wafer, after the semiconductor wafer is separated from the mold.

79. A method of manufacturing the semiconductor device as claimed in claim 77, further comprising cutting the semiconductor wafer along the grid lines to form the independent semiconductor devices after the resin is polished.

80. A method of manufacturing the semiconductor device as claimed in claim 78, further comprising cutting the semiconductor wafer along the grid lines to form the independent semiconductor devices after the resin is polished.

81. A method of manufacturing the semiconductor device as claimed in claim 69, wherein the semiconductor wafer includes back surface opposite to the main surface, and wherein the back surface of the semiconductor wafer is facing to the lower mold having an uneven surface when semiconductor wafer is set in the mold.

82. A method of manufacturing the semiconductor device as claimed in claim 81, wherein the uneven surface is formed in a coarse condition by an electric discharging process.

83. A method of manufacturing the semiconductor device as claimed in claim 82, wherein the area is a first area, the coarse surface is formed within a second area, which is in the first area, and the coarse surface is not formed in the periphery of

the first area.

84. A method of manufacturing the semiconductor device as claimed in claim 83, wherein the coarse surface has a roughness in a range between 8μm and 12μm.

85. A method of manufacturing the semiconductor device as claimed in claim 81, wherein the uneven surface is formed by slits.

86. A method of manufacturing the semiconductor device as claimed in claim 85, wherein the slits are formed in parallel to each other.

87. A method of manufacturing the semiconductor device as claimed in claim 81, wherein the uneven surface is formed by a single spiral slit.

88. A method of manufacturing the semiconductor device as claimed in claim 69, further including buffering stress caused by the lower mold and the upper mold and applied to the semiconductor wafer a shock absorbers during introducing the melted resin on the surface of a semiconductor wafer and during sandwiching the semiconductor wafer

89. A method of manufacturing the semiconductor device as claimed in claim 88, wherein the shock absorbers being disposed symmetrically against the center of

the area.

90. A method of manufacturing the semiconductor device as claimed in claim 89, wherein each shock absorber is formed by a metallic compression spring.

91. A semiconductor wafer, comprising:

semiconductor elements form on a main surface of the semiconductor wafer;

grid lines formed on the main surface of the semiconductor wafer for identifying independent semiconductor devices; and

a resin layer sealing on the main surface of the semiconductor wafer except for on the periphery of the on the main surface of the semiconductor wafer so that the grid lines formed on the periphery of the main surface of the semiconductor wafer is exposed.